Tech-hos

CoaXPress®

Video Interface IP for FPGAs

CoaXPress Overview

- **Supports Video data, control communication, and power supply over single 75Ohm coax cable interface**
- **Video data at 1.25 Gbps - 6.25 Gbps signaling rate (depending on FPGA)**
- **Multi-lane capable for higher bandwidth**
- **Control data at 21 Mbps signaling rate**
- **Cable lengths exceeding 100m without repeaters**
- **Up to 13 Watt power supply per lane**
- **Requires CoaXPress driver or equalizer chip in addition to FPGA Serializer/ Deserializer**
- **For more information on CoaXPress, visit: www.coaxpresss.com**

IP Features

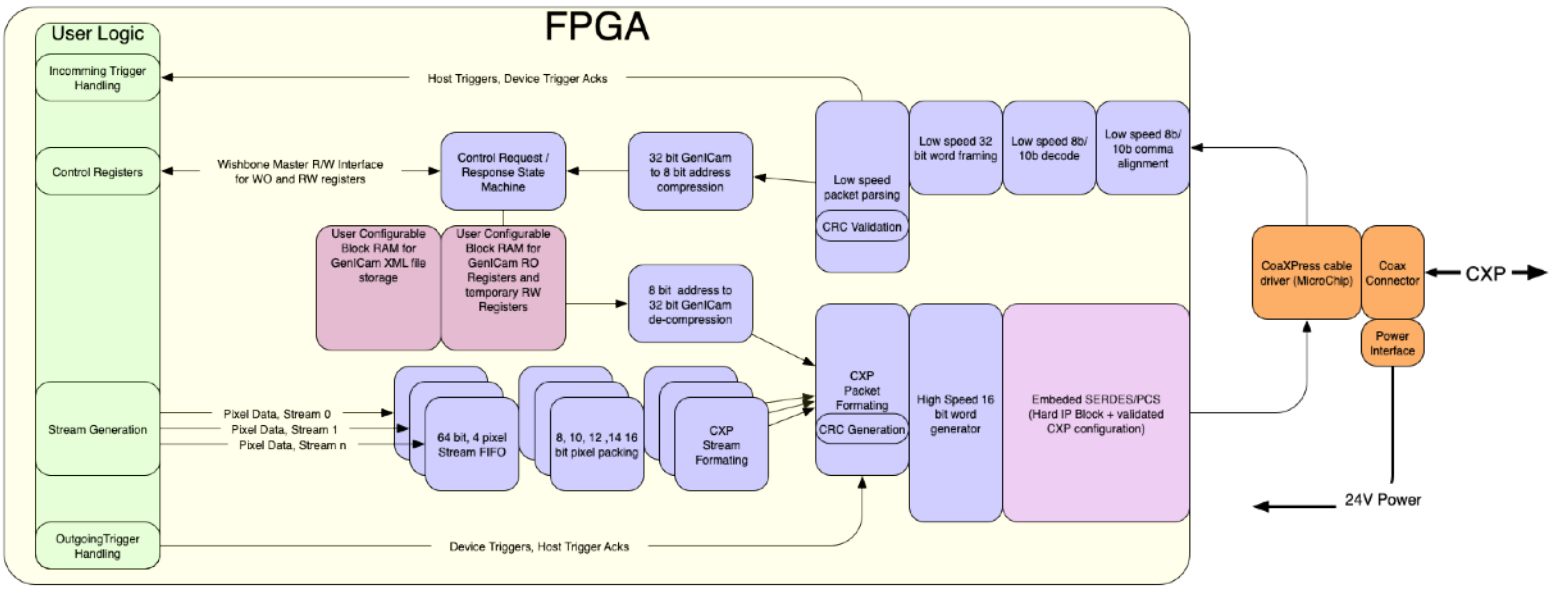
- **Camera (Device) and Frame Grabber (Host) IP sets available**
- **Interfaces with FPGA embedded SERDES/PCS for 1 to 4 high speed lanes**
- **CXP 1, 2, 3, 5, and 6 rates**
- **Full low speed communication lane support**
- **Full GenICam support**
- **Low latency trigger support**
- **Test signaling support**
- **Multi-stream support on single lanes**
- **Wishbone on-chip bus for control features**
- **FIFO-type interfaces for pixel data**
- **PCB layout examples also available**

CoaXPress is a broad standard to facilitate connection between digital video image sources and destinations. In addition to signaling standards, it also includes packet formats, control communication protocols, power management, and many other features.

CoaXPress is a packetized protocol that is more difficult to implement than legacy camera link, SDI, and LVDS interfaces, but provides much greater flexibility in return.

CoaXPress communication is bi-directional but asymmetric to support the highest possible data rates from the video source. This requires completely different logic for CoaXPress devices and hosts. These unique IP systems are packaged and sold separately. Not all CoaXPress requirements can be satisfied by FPGA IP. Support to meet the non-FPGA requirements is also available.

Camera (Device) IP



Not all functions and interfaces are shown in the overview diagram

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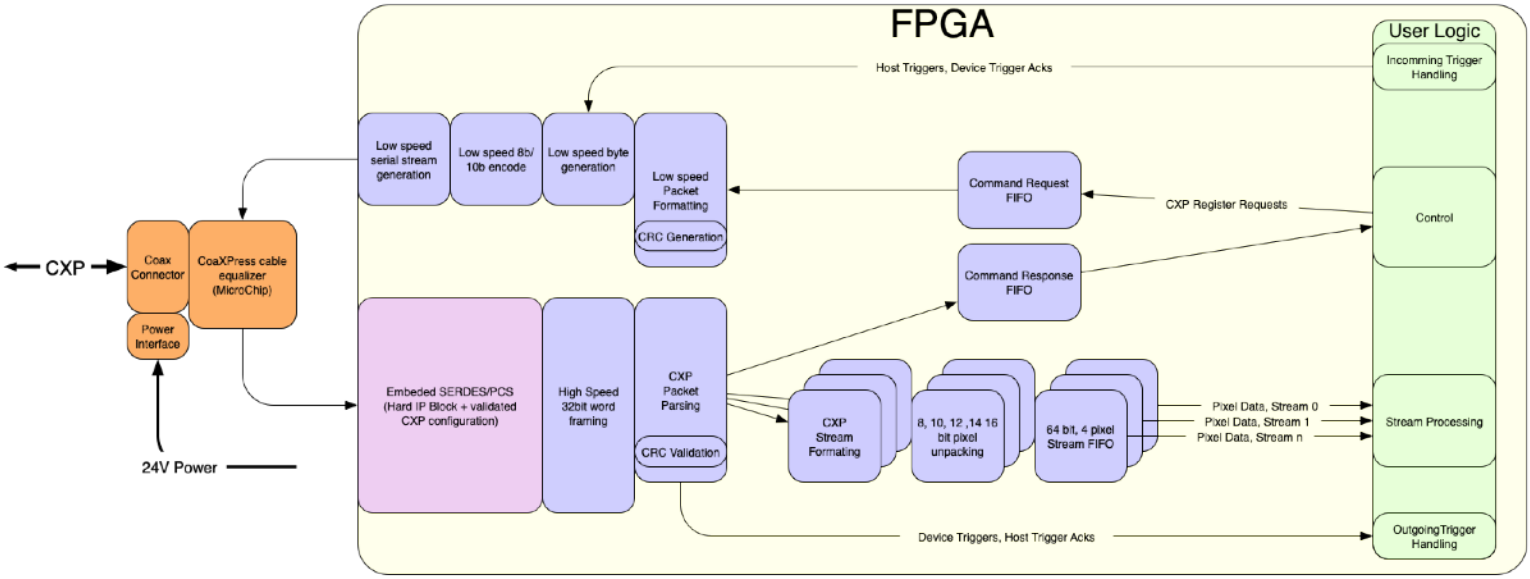
- Self-managed control register transactions only require a Wishbone interface to user configuration registers
- Multi-master, multi-slave, Wishbone logic with integrated register support available for implementation in user logic space
- Multiple transmit streams supported
- Verified configuration for ECP3 SERDES/PCS
- 125MHz reference clock supports CXP 1, 2, 3, 5, and 6
- General purpose logic used for clock recovery, framing, and 8b/10b decode of low speed data
- GenICam-compliant templates available
- Script files included for generating .zipped file for efficient GenICam .xml storage in block RAM
- Automatic CRC generation and validation
- Packet headers automatically generated based on configuration inputs
- Pixel packing included for 8,10,12,14 and 16 bit pixels
- 4 pixel wide data path lowers clock rates along pixel pipeline
- Asynchronous pixel FIFOs support custom clock on user interface
- Individual interfaces for pixel, trigger, and control data
- Outgoing data automatically prioritized, packetized, formatted and delivered
- Incoming data automatically parsed and provided to the user over the appropriate interface

Frame Grabber (Host) IP



Not all functions and interfaces are shown in the overview diagram

- Control register requests and responses supported by command FIFOs
- Multiple incoming pixel streams supported
- Verified configuration for ECP3 SERDES/PCS
- 125MHz reference clock supports CXP 1, 2, 3, 5, and 6
- General purpose logic used for framing and 8b/10b encoding of low speed data
- Automatic CRC generation and validation
- Packet headers automatically verified; metadata provided on module outputs
- Pixel un-packing included for 8,10,12,14 and 16 bit pixels
- Asynchronous pixel FIFOs support custom clock on user interface.
- 4 pixel wide data path lowers clock rates along pixel pipeline
- Separate user interfaces for pixels, triggers, and control data requests / responses
- Incoming packets automatically parsed and their data handled accordingly
- Outgoing data automatically prioritized and appropriately formatted
- Some bit error tolerance implemented for packet header identification